Brochure

Digital VLSI Circuit Design

June 3 – 12, 2017
Organized through NKN
By

Electronics & ICT Academies

IIT Roorkee **IIT Guwahati** **IIITDM Jabalpur** **MNIT Jaipur** **NIT Patna** **NIT Warangal**

Preamble:

"Electronics & ICT Academy" is an initiative of Ministry of Electronics and Information Technology, Govt of India, set up at selected institutes in India. The academies at IIT Guwahati, IIT Roorkee, IIITDM Jabalpur, MNIT Jaipur, NIT Patna and NIT Warangal are jointly organizing a Faculty Development Programme (FDP) on **Digital VLSI Circuit Design during June 3 – 12, 2017**. Experts from IITs, NITs, IIITs and other premier institutes will deliver lectures through National Knowledge Network (NKN) and participants registered at any of the above stated institutes will interactively learn from these lectures. In addition, local course coordinators at respective institutes will take care of practical and practice sessions. Each E&ICT Academy is given with jurisdiction states/UTs in India.

About the Faculty Development Programme (FDP) on Digital VLSI Circuit Design:

The aim of this course is to give a firm foundation in design of custom integrated circuits and standard cells. Transistor sizing and layout are critical to circuit design, which would be taught in this course. Circuit topologies and their timing & power related aspects would also be taught. Impact of layout and transistor sizing on power consumption would be discussed. Rich experience of the speakers at premier institutes will make the participants feel the difference. Exposure and hands-on training with VLSI Design tools will be part of the course.

S.No	Module Name	Topics
1	Fundamental Concepts Module Coordinator - Dr. K S R Krishna Prasad (NIT Warangal)	CMOS fundamentals, Layout and design rules, CMOS inverter
2	Design of Basic Building Blocks Module Coordinator – Dr. P. N. Kondekar (IIITDM Jabalpur)	Combinational logic, Sequential Circuit Elements
3	Concepts for Analysis and Design Module Coordinators - Dr. D. Boolchandani (MNIT Jaipur)	Method of Logical Effort, Timing and Power
4	Multi-Stage Circuits and Subsystems Module Coordinator Dr. Bulusu Anand (IIT Roorkee)	CMOS Memories and Array Structures, Digital CMOS Circuits
5	Soft Skills	Lecture delivery and presentations, holding effective sessions, Handling student questions and queries

Participants are encouraged to list their expectations in their e-mail to the Global Coordinator.

Course Outcomes:

- To understand the functioning, timing and power models of basic CMOS building blocks
- To understand various circuit topologies for implementing combinational, sequential logic and memories
- To understand transistor sizing and layout of different circuit topologies
- Learning EDA tools for schematic entry, layout, extraction and SPICE simulations
- Increase potential of candidates to find job and research opportunities in areas of VLSI, EDA design

Who can apply: The programme is open to faculty of engineering colleges, technical institutions. Limited number of seats may be offered to research scholars depending on availability at E&ICT academies.

Registration Fee Particulars:

Faculty members (General/ OBC) **:Rs. 3,000/- (Three Thousand rupees only)**
Faculty members (SC/ST) **:Rs. 750/- (Seven Hundred Fifty rupees only)**
Persons from Industry **:Rs. 9,000/- (Nine Thousand rupees only)**

Boarding and Lodging will be provided as a part of registration fees by the Academy. No Travel Allowance will be paid to the participants.

Global Coordinator:

Dr. Sanjeev Manhas,
Electronics & Communication Engineering Department
E&ICT Academy
IIT Roorkee
Email: eictiitr@gmail.com, samanfec@iitr.ac.in
Tel: 91-1332-28 6457 (O)

Mode of Payment: Candidate can register either online or offline. For registration, please visit respective E&ICT acdemy website, provided below.

Note: Participants belonging to states not mentioned below can apply to any of the nearest academies as per their choice.

Participants belonging to States/ UTs	Local Coordinator	Contact Details/ website for registration	Payment details (DD / Online transfer)
Telangana, Andhra Pradesh, Karnataka, Goa states and Andaman and Nicobar Islands, Puducherry	Dr P Srihari Rao, **NIT Warangal**	patri@nitw.ac.in http://nitw.ac.in/eict	DD in favor of "Director, NIT Warangal" payable at NIT Warangal or *On-line Mode:* Account Name: Electronics & ICT Academy NITW Account No: 62423775910 and IFSC: SBHY0020149
Assam, Arunachal Pradesh, Manipur, Meghalaya, Mizoram, Nagaland, Tripura, Sikkim	Dr Gaurav Trivedi, **IIT Guwahati**	trivedi@iitg.ernet.in http://www.iitg.ernet.in/eictacad/	DD in favor of "Registrar, IIT Guwahati" Payable at Guwahati or *On-line Mode:* Account Name: IIT Guwahati R&D E&ICT ACADEMY Account No. 36071160089 and IFSC: SBIN0014262
Madhya Pradesh, Chhattisgarh, Maharashtra	Prof. P. N. Kondekar, **IIITDM Jabalpur**	pnkondekar@iiitdmj.ac.in http://ict.iiitdmj.ac.in/	DD in favor of "Electronics and ICT Academy, IIITDMJ" payable at Jabalpur or *On-line Mode:* Account Name: Electronics and ICT Academy, IIITDMJ, Jabalpur Account No. 50302042708 and IFSC: ALLA0212433
Rajasthan, Gujarat, Dadra & Nagar Haveli, Daman & Diu	Dr C Peraswamy, **MNIT Jaipur**	cpsamy.ece@mnit.ac.in http://mnit.ac.in/eict	DD in favor of "Electronics and ICT Academy, MNIT Jaipur" Payable at Jaipur or *Online Mode:* Account Name: Electronics & ICT Academy, MNIT, Jaipur Account No: 676801700483, IFSC: ICIC0006768
Bihar, Jharkhand, Odisha, West Bengal	Dr Gaurav Kaushal, **NIT Patna**	kushalg@nitp.ac.in http://nitp.ac.in/ict/	DD in favor of "Director, NIT Patna" payable at Patna or *On-line Mode:* Account Name: NIT, Patna Account No: 50380476798, IFSC: ALLA0212286
Jammu and Kashmir, Himachal Pradesh, Uttarakhand	Dr Bishnu Prasad Das, **IIT Roorkee**	bpdasfec@iitr.ac.in http://eict.iitr.ac.in/	DD in favor of "Dean SRIC IIT Roorkee" payable at Roorkee or *On-line Mode:* Account Name: Research Project, IIT Roorkee Account No: 33012172097, IFSC: SBIN0001069

Selection: Fifty (50) seats are available at each academy. Participants will be selected based on first-cum-first-serve basis by each academy. Ten (10) more seats are also available for participants from industry. Selected participants will be communicated through e-mail / notified in E&ICT Academy websites.

Important dates:

Last date for submission of application: May 20, 2017
Selection-list intimation/display before: May 27, 2017